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To: Jason Scott Proctor
Art Unit 2123

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Yu-Chin HSU et al

Art Unit: 2123

Application No: 09/829,535

Examiner:
Jason Scott Proctor

Filed: April 9, 2001

For: SYSTEM FOR CHARACTERIZING SIMULATED CIRCUIT LOGIC AND BEHAVIOR

REPLY TO THE OFFICE ACTION MAILED 08/24/2004

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Further examination and consideration of this application are requested in view of the following Amendments and Remarks.

DESCRIPTION AMENDMENTS

Rewrite paragraph [0002] to read as follows:

A circuit designer can model an integrated circuit in several ways. For example FIG. 1 illustrates a schematic diagram modeling one small module MOD1 of an integrated circuit. The schematic diagram models the logic of module MOD1 indicating that it includes AND gates 10-12, OR ~~gates 14-16~~ gates 14-15 and six registers 17- 22 and showing how the parts are interconnected. The schematic diagram also labels the various input, output and internal signals and shows how they are logically related by using symbols to represent OR, AND and register logic operations. While the schematic diagram does not directly indicate how any of the signals the circuit generates would behave in response to particular input signal patterns, it provides enough information to enable a design engineer to determine the signal behavior. However since it is usually hard to figure out how even simple circuits would respond over a long period of time to various input signal patterns, designers normally use computer-based circuit simulators to do the job for them.

Rewrite paragraph [0005] to read as follows:

FIG. 3 is a block diagram illustrating a conventional circuit simulator 23 receiving a netlist 24 and a "test bench" 26 as input and producing an output waveform data 28 describing the behavior of various input, output or internal signals of the circuit modeled by the netlist. The circuit designer typically creates the test bench 26 containing code describing the behavior of the circuit input signals as functions of time and specifying initial states of the circuit's internal data storage elements. Test bench 26 also indicates which circuit input, output and/or internal signals are to be represented by waveform data 28, and specifies parameters controlling the accuracy, duration and other aspects of the simulation. The waveform data 28 ~~simulator 32~~ simulator 23 produces includes a set of data sequences, each representing the magnitude of a separate circuit input, output or internal signal as a function of time.

Rewrite paragraph [0006] to read as follows:

A simulator's output ~~waveform data 38~~ waveform data 28 is often converted into a more comprehensible graphical form when a user 29 wants to view the results of the simulation. Hence most simulators include a display controller 30 for converting waveform data 38 into a waveform display 32 graphically depicting various circuit signals as functions of time.

Rewrite paragraph [0007] to read as follows:

FIG. 4 illustrates an example waveform display 32 that display controller 30 of FIG. 3 could produce from the output waveform data produced by circuit simulator 32 when simulating circuit module MOD1 of FIG. 1. Waveform display 32 illustrates the behavior of register output signals R1-R6, input signals IN1 and IN2 and output signal OUT as functions of time over a period between time 0 and 100 nanoseconds (ns) when clock signal CK1 has a period of 10 ns. Waveform ~~display 28~~ display 32 could also depict the behavior of one or more of the circuits internal signals S1-S5. User 29 (FIG. 3) normally controls the waveform display, for example by telling display controller 30 which waveforms are to be displayed, adjusting the horizontal scale of the waveform display, and choosing the particular span of simulation time depicted in the waveform display.

Rewrite paragraph [0008] to read as follows:

The waveform data output 28 of simulator 23 and waveform display 32 of FIG. 4 are behavioral models of the circuit because they describe the behavior of the signals the circuit generates in response to particular patterns of input signals. However these ~~are logic~~ are not logic models because they do not tell us anything about the structure of the circuit that makes those signals behave that way. Note that the waveform display of FIG. 4 lacks any information about the logic of the circuit module that produced the R1-R6 signals in response to the IN1, IN2 and CK1 signals. Hence a design engineer trying to determine why signal R1 went high instead of staying low at time 90 cannot do so simply by inspecting the waveform display of FIG. 4. He or she must instead return to a logic model of the circuit, such as the schematic model of FIG. 1 or the netlist model of FIG. 2, because those models define the logic relating the behavior of the

various signals. Looking at both the logic model of FIG. 1 and the behavioral model of FIG. 4, the design engineer could determine, for example, that if the R1 signal was to stay low at time 90, then at least one of the R2 and R3 signals should have been low at time 90 when the CK1 signal clocked register 17. The design engineer might also have been able to determine, for example, that the R2 signal would have been low at time 90 if either the R4 signal or the R5 signal had been low at time 80 when the CLK1 signal clocked ~~registers 21 and 22~~ registers 20 and 21.

Rewrite paragraph [00037] to read as follows:

Suppose, for example, that a system user is interested in determining why the R1 signal transitioned from ~~high to low~~ low to high on the CLK1 pulse occurring at time 90. Using a conventional mouse or other pointing device to move a cursor over box 48, the user selects (mouse clicks on) box 48 to highlight it and then clicks on a "FAN_IN" menu item 50 at the top of the display. The system responds by replacing the top level display 38 of FIG. 5 with the lower level display 52 of FIG. 6. Display 52 shows only the box 48 depicting the state change in the R1 signal at time 90 and two other boxes 54 and 55 indicating states of the R2 and R3 signals ~~at times 80~~ at time 80. Note from the schematic diagram of FIG. 1 that between CK1 signal pulses, the R1 signal state is influenced only by the R2 and R3 signal states; the R1 signal following any edge of the CK1 signal is the logical AND of the R2 and R3 signals following the preceding edge of the CK1 signal. State changes in no other signals can affect the state of the R1 signal between CLK1 signal pulses.

Rewrite paragraph [00040] to read as follows:

The user may then highlight the ~~R4 box 57~~ R3 box 55 of FIG. 7 and again click the FAN-IN button 50 (FIG.1) to tell the system to produce display 67 of FIG. 8. Display 67 expands display 56 of FIG. 7 by including another icon 66 and boxes 68 indicating states of signals R1 and R5 at time 70 which influence the state of the R3 signal at time 80. By highlighting various boxes of FIG. 8 and again clicking the FAN-IN button, the user can tell the system to further expand the

display as illustrated in FIG. 9 to include another set of boxes and icons 72 indicating states of various signals at time 60 that influence the states of signals R1, R4 and R5 at time 70.